

Remarks

Claims 1, 2, 6-11, 13-15, 18, and 19 are currently pending in the present application. The Applicants have amended Claims 1, 2, 6, 8, and 9. Support for these claim amendments may be found, for example, at paragraphs [0029]-[0033] and at Figs. 3-5 of the Specification. In view of the foregoing amendments and following remarks, reconsideration and withdrawal of the 35 U.S.C. §103 grounds of rejection is respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 1, 2, 6-11, 13-15, 18, and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,720,850 to Sasabata et al., hereinafter “Sasabata”, in view of U.S. Patent No. 6,518,823 to Kawai, hereinafter “Kawai”. For the reasons set forth below, the Applicant respectfully submits that Claims 1, 2, 6-11, 13-15, 18, and 19 are fully patentable over the theoretical combination of Sasbata and Kawai.

Claim 1 as amended recites:

An integrated circuit switch comprising: at least two signal ports coupled by a signal path, the signal path including a channel of at least one series FET; a shunt path coupled to ground and including a channel of a shunt FET; a first control voltage applied to the signal path; and, a second control voltage applied directly to both to a gate terminal of the series FET and to a drain terminal of the shunt FET, wherein the second control voltage, the drain terminal of the shunt FET, and the gate terminal of the series FET are directly and continuously coupled to each other.

As emphasized above, Claim 1 recites a switching device comprising at least one series FET and a shunt FET. (see Figure 3 of the Specification). As explained prior Responses (April 21, 2006; September 14, 2005), important to the claimed configuration is the drain terminal of the shunt FET being directly coupled to the gate of the series FET. In the instant Response, Claim 1 has been amended to better describe the relationship between the series FET, the shunt FET, and the second

control voltage. Independent Claims 2, 6, 8, and 9 have been similarly amended. Support for these claim amendments may be found, for example, at Figs. 3, 5, and 5 of the Specification.

The direct (*and continuous*) coupling between the second control voltage, the drain terminal of a shunt FET, and the gate of a series FET enables a single control signal to have the opposite effect on each of the FETs (i.e., turning one ON when the other is OFF, and vice versa), and to thus permit a common logic signal to control both transistors (see page 7, paragraphs [0029]-[0030] of the Specification). Indeed, if this recited configuration were replaced with a switch, as suggested by the June 20, 2006 Office Action, a single control signal would not be able to simultaneously turn one transistor ON while turning another transistor OFF, and vice versa. (emphasis added).

Nonetheless, the Office Action asserts that applying a voltage source to one of two CMOS transmission gates 61, 62 in a semi-conductor switch 52 (Kawai) enables one transmission gate to be turned ON while simultaneously turning OFF a series FET (connected to the switch 52), and vice versa. The Office Action, however, provides no factual evidence in support of such an assertion. It is the Applicant's understanding, (assuming, *arguendo*, that a CMOS transmission gate is equivalent to a shunt FET), that applying voltage to a switch, so as to turn ON one of the switch's transmission gates, will result in turning ON a series FET coupled to the switch. As noted above, this is the exact opposite effect recited in the claims. Accordingly, the Applicant respectfully requests that the PTO provide either factual evidence or an Affidavit of Official Notice, in accordance with 37 C.F.R. 1.104(d)(2), with respect to the assertion described above.

The Applicant now briefly describes the Sasabata and Kawai references cited in the June 20, 2006 Office Action. Sasabata relates to a single-pole double-throw (SPDT) switch for use in providing attenuation to a high-frequency signal during conduction. In particular, Sasabata discloses

a SPDT switch 41 comprising series FETs, 43, 46, a constant voltage source 50 connected to the sources of FETs 43 and 46, and a variable-voltage generator 52 connected to the gates of FETs 43 and 46. (see Figure 5 and column 9, line 40 to column 10, line 8 of Sasabata). The variable-voltage generator 52 "...switches between a voltage V_{α} ... and V_{cc} , thereby feeding the voltage V_{α} or V_{cc} to the gates of FETs 43 and 46". (emphasis added). (see column 10, lines 4-8 of Sasabata).

As indicated by in the June 20, 2006 Office Action, Sasabata fails to disclose a shunt FET wherein a drain terminal of the shunt FET is directly coupled to a gate terminal of a series FET. The Office Action proposes, however, that replacing the switch within the semi-conductor circuit 52 of Sasabata with a transmission gate structure 52 taught in Kawai yields a shunt FET structure equivalent to the shunt FET as claimed. To this, the Applicants respectfully disagree, particularly since Kawai also fails to disclose a shunt FET, or an equivalent thereto.

Referring now to Kawai, Kawai discloses an integrated circuit in which a one-time programmable logic device disables writing to a storage device once a current is passed therethrough. (see Abstract of Kawai). In particular, with regards to Figures 7 and 8, Kawai discloses a semi-conductor switch 52 having a contact 52a connected to a fuse 18, a fixed contact 52b connected to output of a SUR circuit 16, a second fixed contact 52c connected to a pad 22 and external power supply 24, and a switching control terminal 52d connected to a pad 54 serving as an internal terminal for reading/writing control. (see Kawai at column 7 lines 51-64). This semi-conductor switch 52 further comprises transmission gates 61 and 62, each formed by a CMOS transistor with small power consumption and an inverter 63. (see column 8, lines 54-58 of Kawai).

As indicated above, the Office Action suggests combining the semi-conductor switch 52 taught by Kawai with the SPDT switch 41 of Sasabata. In support of such a combination, the Office

Action again asserts that the semi-conductor switch 52 of Kawai, (which comprises two transmission gates 61, 62 (each formed by a CMOS)), is equivalent to the single shunt FET recited in the claims. This assertion is particularly troublesome since it is the Applicants understanding that each CMOS in the Kawai switch 52 is itself comprised of a series of transistors. Nonetheless, the Office Action continues to maintain the equivalency between a switch 52 comprising two CMOS gates and a single shunt FET. The Office Action fails, however, to provide factual evidence in support of such an assertion. Accordingly, the Applicant respectfully requests that the PTO provide either factual evidence or an Affidavit of Official Notice, in accordance with 37 C.F.R. 1.104(d)(2), with respect to the assertion that a semi-conductor switch 52 comprising two CMOS gates is equivalent to a single shunt FET.

Furthermore, even if, *arguendo*, the switch 52 of Kawai were equivalent to the single shunt FET recited in the present application, the Office Action has failed to provide a proper motivation for combining the switch 52 of Kawai with the circuit of Sasabata. Instead, the Office Action simply asserts "...[t]he motivation for using such a structure as that disclosed in Kawai is simply to obtain the well-known advantages associated with such a transmission gate structure..." This assertion, however, is not supported by any evidence, as required by law.

To establish a *prima facie* case of obviousness, three basic criteria must be met: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art reference (or references when combined) must teach or suggest all the claim limitations. See, M.P.E.P. 2142 (Eighth Edition, Feb. 2003).

As a threshold matter, there must be some teaching, suggestion or motivation in the prior art to make the specific change made by the applicant. In re Dance, 160 F.3d 1339, 1343 (Fed. Cir. 1998). Obviousness should be measured “at the time the invention was made” (i.e. the filing date of the application), and with no prior knowledge of the applicant’s disclosure. In re Dembiczak, 175 F.3d 994, 998-999 (Fed. Cir. 1999).

Obviousness cannot be established by a hindsight combination to produce the claimed invention. In re Dance, 160 F.3d. at 1343. The Examiner must show reasons why the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the prior art references for combination in the manner claimed. In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998).

In the present case, the Office Action has failed to identify evidence in support of a motivation, teaching or suggestion in either Kawai or Sasabata which would have lead one of ordinary skill in the art to combine the switch 52 of Kawai with the circuit if Sasabata. Indeed, the Office Action concedes that no such teaching or suggestion is disclosed. Nonetheless, the Office Action maintains that one skilled in the art would have been motivated to substitute Sasabata’s circuit with the Kawai switch. The Office Action, however, fails to provide actual evidence in support of such an alleged motivation. Instead, it is believed that the Official Action inadvertently relied on impermissible hindsight to piece together the elements recited in the claims using the Applicants’ own disclosure as a roadmap.

A proper obviousness analysis requires the difficult but critical step of casting the mind back to the time the invention was made. It is this requirement that guards against entry into the “tempting but forbidden zone of hindsight”. *In re Dembiczak*, 50 USPQ2d 1614, 1616-17 (Fed Cir

1999). To this end, the Court in Dembiczak made clear that the “best defense against the subtle but powerful attraction of hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.” *Id.* The evidence of a suggestion, teaching or motivation to combine references can come from a number of sources; but the range of sources available “does not diminish the requirement for actual evidence.” (emphasis added). *Id.*

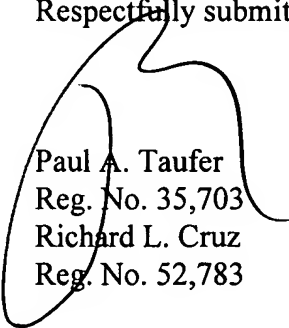
Accordingly, since the Office Action fails to provide any actual evidence in support of its alleged motivation, the Applicants respectfully submit that there is no proper suggestion or motivation to combine the switch (52) with the circuit of Sasabata.

In sum, the Applicant submits that the theoretical combination of Sasabata and Kawai fails to disclose an equivalent structure to that recited in the claims, particularly because a multi-gate CMOS switch is neither structurally nor functional equivalent to a shunt FET. Furthermore, even if, *arguendo*, the Kawai switch were equivalent to a shunt FET, the Sasabata-Kawai combination fails to disclose the direct and continuous coupling between a voltage source, the gate of a series FET, and the drain of a shunt FET. Thirdly, since the Office Action fails to provide a proper motivation for combining Sasabata and Kawai, the theoretical combination may not be the basis for an obviousness rejection. Accordingly, the Applicant respectfully submits that independent Claims 1, 2, 6, 8, and 9 are fully patentable over the theoretical combination of Sasabata-Kawai, and respectfully requests reconsideration and withdrawal of the §103 grounds of rejection.

Conclusion

In view of the foregoing amendments and remarks, the Applicant submits that the present Application, including Claims 1, 2, 6-11, 13-15, 18 and 19, is now in condition for allowance. A indication reflecting the same is earnestly solicited.

Respectfully submitted,



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